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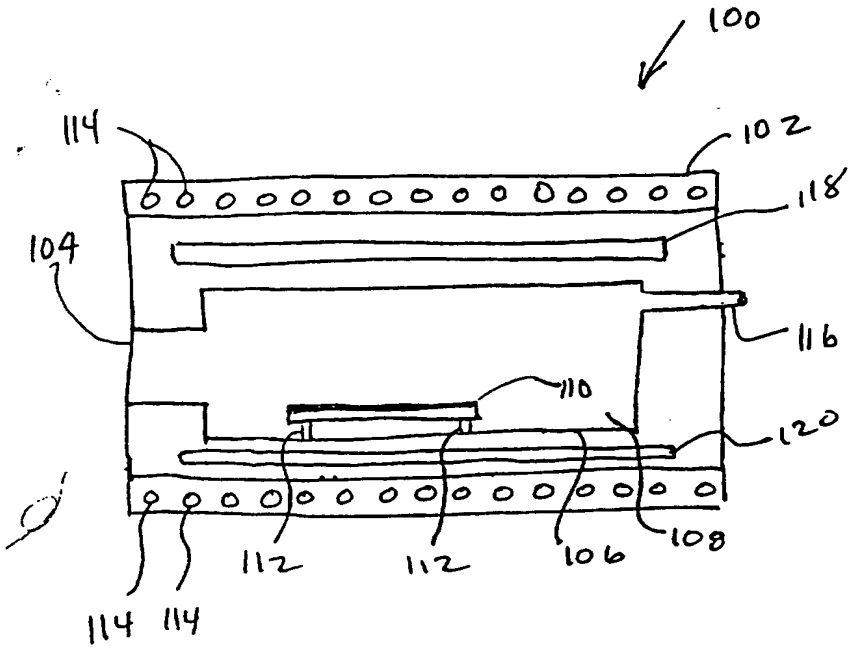
(54) Title: GAS ASSISTED RAPID THERMAL ANNEALING



(57) Abstract: An improved method for rapid thermal processing of a semiconductor wafer. The method adds a significant conductive heat transfer component to a semiconductor process, which changes the temperature of a semiconductor wafer. The method can include the introduction of a thermally conductive gas, such as He or H_2, into the processing chamber during processing of a semiconductor wafer. Once the wafer is disposed in the chamber, the thermally conductive gas acts to conduct heat from the walls of the chamber to the wafer surface, to heat the wafer. Alternatively, as the wafer is removed from the hot processing chamber and moved into an adjoining loadlock, the thermally conductive gas can act as a heat transfer conduit between the hot wafer and the relatively cooler walls of the loadlock to cool the wafer.

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GAS ASSISTED RAPID THERMAL ANNEALING

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to semiconductor manufacturing equipment and, more particularly, to an improved method for rapid thermal processing of a semiconductor wafer.

2. Description of Related Art

In the semiconductor manufacturing industry, depending upon the particular process, a semiconductor wafer may be treated at temperatures of from about 100° C to about 1300° C, under controlled conditions, in rather sophisticated furnaces. Commonly, these furnaces are horizontal or vertical type furnaces, which use various energy sources to heat the wafer, including radiant heaters, arc lamps, and tungsten-halogen lamps. As shown in FIG. 1, a typical horizontal or vertical type furnace requires a time t_1 for ramping up to a particular process temperature to process the wafers. The ramp up rate for a typical furnace is usually between 5 °C/min to about 15 °C/min, which makes time t_1 typically on the order of about 1 hour. A time t_2 is required for cooling of the wafers, which is generally on the order of about 2 hours. Long processing times are typically unacceptable in advanced semiconductor device manufacturing because of dopant redistribution, excessive costs, excessive exposure to temperature, and high power requirements.

In order to continue to make advancements in the development of semiconductor devices, especially semiconductor devices of decreased dimensions, new processing and manufacturing techniques have been developed. One such processing technique is know as Rapid Thermal Processing (RTP), which reduces the amount of time that a semiconductor device is exposed to high temperatures during processing. The rapid thermal processing technique, typically includes raising the temperature of the wafer and holding it at that temperature for a time long enough to successfully

perform a fabrication process, and avoid such problems as unwanted dopant diffusion that would otherwise occur at the high processing temperatures.

FIG. 2 schematically illustrates a typical "cold-wall" RTP unit 2, having a wafer 4, which is heated by radiation, using a plurality of high intensity lamps 6. The radiation energy is usually transmitted through a quartz window 8. As in most forms of wafer processing, temperature uniformity across the wafer is a primary design consideration. Difficulties arise in achieving temperature uniformity when the temperature of the wafer is increased using primarily radiant heat transfer in a "cold-wall" furnace. Unfortunately, much of the heat energy is used to raise the temperature of the furnace walls, quartz windows, and wafer insertion equipment. Moreover, since over a period of the processing time, the wafer temperature is greater than that of the chamber walls, heat tends to be conducted away from the wafer making it more difficult to heat the wafer.

SUMMARY OF THE INVENTION

The present invention provides an improved method and structure for rapid thermal processing of a semiconductor wafer. The improved method helps to improve process times so as to avoid, for example, the creation of thermal gradients in the process chamber, which can cause slip and warpage of the wafer. The method adds a significant conductive heat transfer component to processes which may presently use primarily radiant heat transfer to raise the temperature of a semiconductor wafer. The method includes the introduction of a thermally conductive gas, such as He or H_2, or gases containing He or H_2, into the processing chamber during processing. As shown in FIG. 3, He and H_2 are examples of gases having high thermal conductivity relative to gases such as air, N_2, O_2, and Argon, across a wide range of process temperatures. Thus, He and H_2 or gases containing these elements are examples of gases preferably suited for use in the present invention.

In one aspect of the present invention, a method is provided for processing a semiconductor device. The method includes providing a processing chamber having an inner chamber surface, which defines a cavity configured to receive a semiconductor device. Next a thermally conductive gas is introduced into the processing chamber. Heat is conducted through said

thermally conductive gas to change the temperature of the semiconductor device.

In another aspect of the present invention, an apparatus for processing a semiconductor device is provided. The apparatus includes a processing chamber, which has an inner chamber surface defining a cavity configured to receive a semiconductor device. The apparatus also includes a means for introducing a thermally conductive gas into the processing chamber. The thermally conductive gas conducts heat to and from the semiconductor device to change the temperature of the semiconductor device.

These and other features and advantages of the present invention will be more readily apparent from the detailed description of the preferred embodiments set forth below taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a graph representative of typical temperature heat-up and cool-down rates for a conventional wafer processing furnace;

FIG. 2 is a simplified illustration of a typical cold-wall RTP unit;

FIG. 3 is a graph showing typical thermal conductivity properties of selected gases over a range of temperatures;

FIGS. 4A and 4B illustrate schematically a side view and top view, respectively, of one embodiment of a semiconductor wafer processing system in accordance with the present invention;

FIG. 5 is a simplified cross-sectional illustration of an embodiment of a reactor in accordance with the present invention;

FIG. 6A is a simplified cross-sectional illustration of another embodiment of a reactor in accordance with the present invention;

FIGS. 6B and 6C are a top and side view, respectively, of a component of the reactor in FIG. 6A;

FIG. 7 illustrates of yet another embodiment of the reactor of the present invention;

FIG. 8 is a flow diagram of an embodiment of a process of the present invention; and

FIG. 9 is a graph comparing wafer temperature as a function of time between a wafer disposed in the pre-heated chamber in air and a wafer disposed in the pre-heated chamber in He in accordance with principles of the present invention.

DETAILED DESCRIPTION

FIGS. 4A and 4B illustrate schematically a side view and top view, respectively, of one embodiment of a semiconductor wafer processing system 10 that establishes a representative environment of the present invention. Processing system 10 includes a loading station 12 which has multiple platforms 14 for supporting and moving a wafer cassette 16 up and into a loadlock 18. Wafer cassette 16 may be a removable cassette which is loaded onto a platform 14, either manually or with automated guided vehicles (AGV). Wafer cassette 16 may also be a fixed cassette, in which case wafers are loaded onto cassette 16 using conventional robots or loaders (not shown). Once wafer cassette 16 is inside loadlock 18, loadlock 18 and transfer chamber 20 are maintained at atmospheric pressure or else are pumped down to a vacuum pressure using a pump 50. A robot 22 within transfer chamber 20 rotates toward loadlock 18 and picks up a wafer 24 from cassette 16. A reactor or thermal processing chamber 26, which may also be at atmospheric pressure or under vacuum pressure, accepts wafer 24 from robot 22 through a gate valve 30. Optionally, additional reactors may be added to the system, for example reactor 28 located vertically beneath chamber 26 to save floor space. Embodiments of reactor 26 in accordance with the present invention are described in greater detail below. Robot 22 then retracts its arm which carried wafer 24 and, subsequently, gate valve 30 closes to begin the processing of wafer 24. After wafer 24 is processed as described below, gate valve 30 opens to allow robot 22 to pick-up and place wafer 24 into cooling station 60. Cooling station 60 cools the newly processed wafers before they are placed back into a wafer cassette in loadlock 18.

FIG. 8 is a flow diagram of an embodiment of a process 300 of the present invention. In this embodiment, a process chamber is provided and ramped up to a process temperature (310). A wafer is loaded into the chamber (312). The wafer may be loaded either before or after the inner chamber has reached a steady-state temperature. Next, a thermally conductive gas is

introduced into the heated process chamber (314), such that the gas can contact the hot inner walls of the process chamber and the wafer surface. Alternatively, the thermally conductive gas may be introduced into the process chamber after the wafer is loaded into the process chamber and while the temperature is ramping-up. This alternative embodiment creates a more uniform temperature distribution through the process chamber. The thermally conductive gas conducts heat from the walls and structures of the process chamber to heat the wafer. In one embodiment, the thermal conductive gas may be H_2 or He or any gas containing H_2 or He. Thus, the H_2 or He gas concentration may range from 0.1% to 100 %. In conjunction with the radiant heat transfer in the process chamber, the conductive heat transfer causes the temperature of the wafer to rise much more rapidly. Conversely, as the wafer is removed from the hot processing chamber (318) and moved to an adjoining cooling station, the thermally conductive gas can enter the transfer chamber and act as a heat transfer conduit between the hot processed wafer and the relatively cooler walls of the transfer chamber, which acts to cool the wafer.

Referring again to FIGS. 4A and 4B, reactor 26 may be any type of "hot-wall" reactor which allows wafers to be loaded at wafer processing temperatures, of between about 100° to about 1200°c, without adverse results. In accordance with the present invention, the reactor may be a hot-walled RTP reactor, such as is used in thermal anneals. In other embodiments, the reactor may be the type of reactor used for dopant diffusion, thermal oxidation, nitridation, chemical vapor deposition, and/or similar processes. The reactor is bolted onto transfer chamber 20 and is further supported by a support frame 32. Process gases, coolant, and electrical connections may be provided through the rear end of the reactors using interfaces 34.

FIG. 5 is a simplified cross-sectional illustration of an embodiment of a reactor 100 in accordance with the present invention. Reactor 100 may generally include a closed-end process chamber 106, which defines an interior cavity 108. Process chamber 106 may be constructed with a substantially rectangular cross-section, having a minimal internal volume surrounding wafer 110. In an exemplary embodiment, the volume of process chamber 106 may be no greater than 5000 cm^3, preferably less than about 3000 cm^3. One result of the small volume is that uniformity in temperature is more easily maintained. Additionally, the small process chamber volume allows reactor 100 to be made smaller, and as a result, processing system 10 may be made

smaller, requiring less clean room floor space. Process chamber 106 may be made of aluminum, quartz or other suitable material, such as silicon carbide or Al_2O_3. To conduct a process, process chamber 106 should be capable of being pressurized. Typically, process chamber 106 should be able to withstand internal pressures of about 0.001 Torr to 1000 Torr, preferably between about 0.1 Torr and about 760 Torr.

Within process chamber 106 are wafer support standoffs 112, which support the single wafer 110. Standoffs 112 may be any high temperature resistant material, such as quartz, and may have a height of between about 50 μm and about 20 mm.

Opening 104, shown at the left end of process chamber 106, provides access for the loading and unloading of wafer 110 before and after processing. Opening 104 may be a relatively small opening, but with a height and width large enough to accommodate a wafer of between about 0.5 to 2 mm thick and up to about 300 mm (~12 in.) in diameter, and the arm of robot 22 passing therethrough. The height of opening 104 is no greater than between about 18 mm and 50 mm, and preferably, no greater than 20 mm. The relatively small opening size helps to reduce radiation heat loss from process chamber 106, and keeps down the number of particles entering cavity 108 to allow for easier maintenance of the isothermal temperature environment.

In this embodiment, a plurality of heating elements 114 surround a top and a bottom portion of process chamber 106. Resistive heating elements 114 may be disposed in parallel across chamber 106 such that each element 114 is in relative close proximity to each other element 114. For example, each resistive heating element 114 may be spaced between about 5 mm and 50 mm apart; preferably between about 10 mm and 20 mm apart. Accordingly, the close spacing of heating elements 114 provides for an even heating temperature distribution across the wafer positioned in cavity 108. Resistive heating element 114 may include a resistive heating element core and a filament wire. The core is usually made of a ceramic material, but may be made of any high temperature rated, non-conductive material. The filament wire is conventionally wrapped around the core to allow an optimal amount of heat energy to radiate from the element. The filament wire may be any suitable resistively heatable wire, which is made from a high mass material for increased thermal response and high temperature stability, such as SiC, SiC coated

graphite, graphite, NiCr, AlNi and other alloys. Preferably, the resistive heating filament wire is made of a combination Al-Ni-Fe material, known commonly as Kantal A-1 or AF, available from Omega Corp. of Stamford, Connecticut.

A direct line voltage of between about 100 volts and about 500 volts may be used to power the resistive elements. Thus, in this embodiment no complex power transformer is needed for controlling the output of resistive heating elements 114.

Optionally, reactor 100 includes heat diffusing members 118 and 120, which are positioned proximate to and typically overlay heating elements 114. Heat diffusing members 118 and 120 absorb the thermal energy output from heating elements 114 and dissipate the heat evenly within chamber 106. It should be appreciated that by heating wafer 110 from above and below, and further by keeping the distance between heat diffusing members 118 and 120 small, the temperature gradient within chamber 106 is more easily isothermally maintained. For example, if top heat diffusing member 118 is maintained at 1000°C and bottom heat diffusing member 120 is also maintained at 1000°C, the temperature in the small space between them should also be substantially maintained at 1000°C with very little fluctuation. Heat diffusing members 118 and 120 may be any suitable heat diffusing material that has a sufficiently high thermal conductivity, preferably Silicon Carbide, Al_2O_3, or graphite. Reactor 100 is fully disclosed in co-pending U.S. Patent Application Serial No. 09/451, 494, filed November 30, 1999, which is herein incorporated by reference for all purposes.

FIG. 6A is a simplified illustration of yet another embodiment of a reactor in accordance with the present invention. In this embodiment, reactor 200 includes a process chamber 212, similar to that shown in FIG. 5, and a heating assembly 218. Heating assembly 218 includes heating member or plate 220, at least one heat source 222, and a coupling mechanism 224. In a preferred embodiment, heating assembly 218 may be positioned suspended within process chamber 212, in a cantilevered relationship on a wall of process chamber 212. Alternatively, heating assembly 218 may rest on mounts emanating up from a floor of process chamber 212.

As shown in FIG. 6B and 6C, heating plate 220 of heating assembly 218 may have a large mass relative to wafer 216, and may be fabricated from a

material, such as silicon carbide, quartz, inconel, aluminum, steel, or any other material that will not react at processing temperatures with any ambient gases or with wafer 216. Arranged on a top surface of heating plate 220 may be wafer supports 226. In a preferred embodiment, wafer supports 226 extend outward from the surface of heating member 220 to support the single wafer 216. Wafer supports 226 are sized to ensure that wafer 216 is held in close proximity to heating member 220. For example, wafer supports 226 may each have a height of between about 50 μm and about 20 mm, preferably about 2 mm to about 8 mm. The present invention includes at least three wafer supports 226 to ensure stability. However, the total area of contact between wafer supports 226 and wafer 216 is less than the size of the wafer, preferably less than about 300 mm^2.

Heating plate 220 may be formed into any geometric shape, preferably a shape which resembles that of the wafer. In a preferred embodiment, heating plate 220 is a circular plate. The dimensions of heating plate 220 may be larger than the dimensions of wafer 216, such that the surface area of the wafer is completely overlaid by the surface area of heating plate 220. As illustrated in FIG. 6A, the diameter of heating plate 220 may be no less than the diameter of wafer 216; preferably, the diameter of heating plate 220 is greater than the diameter of wafer 216. For example, the radius of heating plate 220 is greater than the radius of wafer 216 by about a length γ, which is between about 1 mm and 100 mm, preferably 25 to 50 mm.

On a periphery of heating plate 220 is at least one heat source 222. Heat source 222 may be a resistive heating element or other conductive/ radiant heat source, which can be made to contact a peripheral portion of heating plate 220 or may be embedded within heating plate 220. The resistive heating element may be made of any high temperature rated material, such as a suitable resistively heatable wire, which is made from a high mass material for increased thermal response and high temperature stability, such as SiC, SiC coated graphite, graphite, AlCr, AlNi and other alloys. Resistive heating elements of this type are available from Omega Corp. of Stamford, Connecticut.

Coupling mechanism 224 includes a mounting bracket 228 and electrical leads 230 to provide an electrical power connection to heat source 222. Mounting bracket 228 is coupled to an internal wall of process chamber 212 using conventional mounting techniques. Once mounted, electrical leads 230

can extend outside of process chamber 212 to be connectable to an appropriate power source. The power source may be a direct line voltage of between about 100 volts and about 500 volts.

FIG. 7 is an illustration of yet another embodiment of the reactor of the present invention. Referring to FIGS. 6A-6C and 7 a plurality of heating members 220 may be stacked together within process chamber 212. In a preferred embodiment, mounting holes 232 (Fig. 6A) are provided on a periphery of each heating member 220 and extend therethrough. Any appropriate number of mounting holes may be used to ensure that each heating member 220 is supported. In one embodiment, a rod 234 or similar structure may be threaded through mounting holes 232 and spacers 236. Spacers 236 keep each heating member 220 an appropriate distance away from each other heating member 220, which ensures that wafer supports 226 and wafer 216 can be fit in-between stacked heating members 220. As best understood with reference to FIG. 6B, each mounting hole 232 is positioned on the half of heating member 220 nearest coupling mechanism 224. In this manner, the half of heating member 220 toward where the loading/unloading of wafer 216 occurs, is free of spacers 236. This arrangement ensures that the loading/unloading of wafer 216 onto each heating member 220 is not impeded. Preferably, the distance between the stacked heating plates may be between about 10 mm and 50 mm, more preferably about 20 mm. The top most stacked heating member 220(designated as heating member 238) may be the same in structure and function as each other heating member 220, except that the top most heating member 238 may not have a wafer placed upon it.

As can be best understood from FIG. 7, in the stacked arrangement, wafer 216 can be heated from top and bottom, which may provide a more uniform and consistent heating environment across the wafer.

FIG. 9 shows experimental data of wafer temperature as a function of time between a 200 mm wafer disposed in the pre-heated chamber in air and a 200 mm wafer disposed in the pre-heated chamber in He. For example, the temperature of the wafer disposed in He rises to 300°C in about 35 seconds of processing time. The wafer in air requires more than about 100 seconds of processing time to reach a temperature of 300°C. Thus, the present invention

reduces wafer processing times, which can help increase wafer throughput and decrease processing costs.

Having thus described embodiments of the present invention, persons skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention. Thus the invention is limited only by the following claims.

WHAT IS CLAIMED IS:

1. A method for processing a semiconductor device, the method comprising:

providing a processing chamber having an inner chamber surface defining a cavity configured to receive a semiconductor device therein;

introducing a thermally conductive gas into said processing chamber; and

conducting heat through said thermally conductive gas to change the temperature of said semiconductor device.

2. The method of Claim 1, further comprising radiating heat from said inner chamber surface to change the temperature of said semiconductor device.

3. The method of Claim 1, wherein said process chamber comprises a rapid thermal processing (RTP) chamber.

4. The method of Claim 1, wherein said inner chamber surface is heated with a resistance heating element to a selected processing temperature.

5. The method of Claim 1, wherein said heating of said semiconductor device occurs at a rate of about 50 °C/min.

6. The method of Claim 1, wherein said thermally conductive gas is taken from the group consisting of He gas, H_2 gas, and gas mixtures containing He gas and H_2 gas.

7. The method of Claim 1, wherein said thermally conductive gas has a thermal conductivity greater than the thermal conductivity of N_2 and O_2.

8. The method of Claim 1, wherein said pressure in said processing chamber is between about 0.001 Torr and 1000 Torr.

9. A method for processing a semiconductor wafer, the method comprising:

providing a rapid thermal processing chamber having a resistance heated wall defining a cavity capable of receiving said wafer; and

introducing a thermally conductive gas into said rapid thermal processing chamber; and

conducting heat through said thermally conductive gas between said resistance heated wall and said wafer to vary the temperature of said wafer.

10. The method of Claim 9, further comprising heating said wafer through radiation of heat from said resistance heated wall.

11. The method of Claim 9, wherein said temperature of said wafer varies at a rate of about 50 °C/min.

12. The method of Claim 9, wherein said thermally conductive gas has a thermal conductivity greater than the thermal conductivity of air, N_2 and O_2.

13. The method of Claim 9, wherein said thermally conductive gas is taken from the group consisting of He gas, H_2 gas, and gas mixtures containing He gas and H_2 gas.

14. The method of Claim 9, wherein said pressure in said processing chamber is between about 0.001 Torr and 1000 Torr.

15. The method of Claim 9, further comprising cooling said wafer by conducting heat through said thermally conductive gas between said wafer and a wall.

16. An apparatus for processing a semiconductor device, the apparatus comprising:

a processing chamber having an inner chamber surface defining a cavity configured to receive a semiconductor device therein; and

means for introducing a thermally conductive gas into said processing chamber, said thermally conductive gas conducting heat to and from said semiconductor device to change the temperature of said semiconductor device.

17. The apparatus of Claim 16, wherein said process chamber comprises a rapid thermal processing (RTP) chamber.

18. The apparatus of Claim 16, wherein said heating of said semiconductor device occurs at a rate of about 50 °C/min.

19. The apparatus of Claim 16, wherein said thermally conductive gas is taken from the group consisting of He gas, H_2 gas, and gas mixtures containing He gas and H_2 gas.

20. The apparatus of Claim 16, wherein said thermally conductive gas has a thermal conductivity greater than the thermal conductivity of N_2 and O_2.

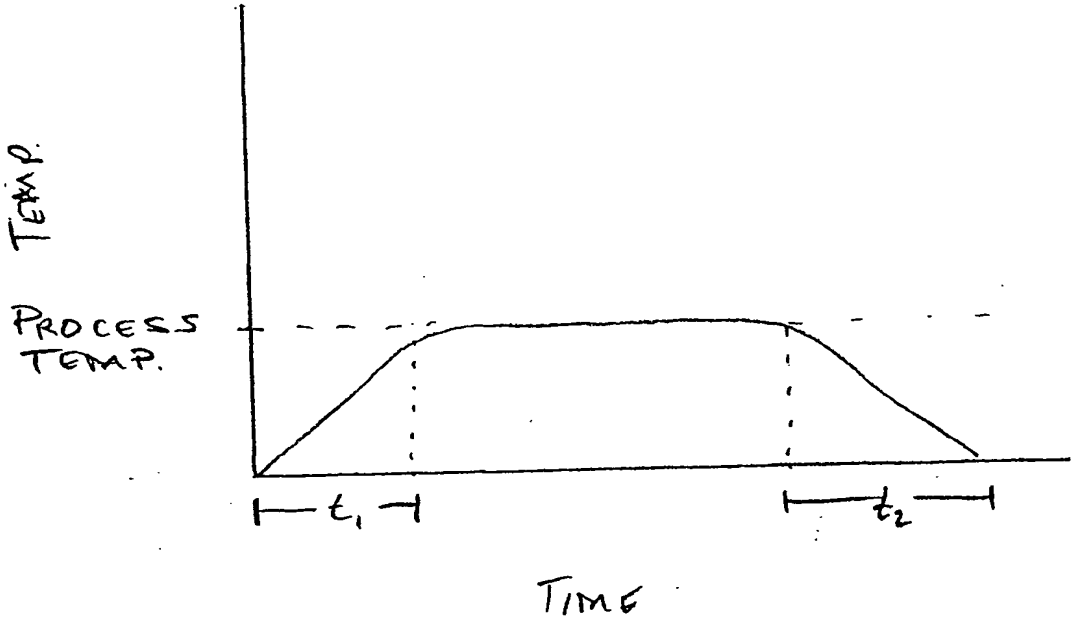


FIG_1

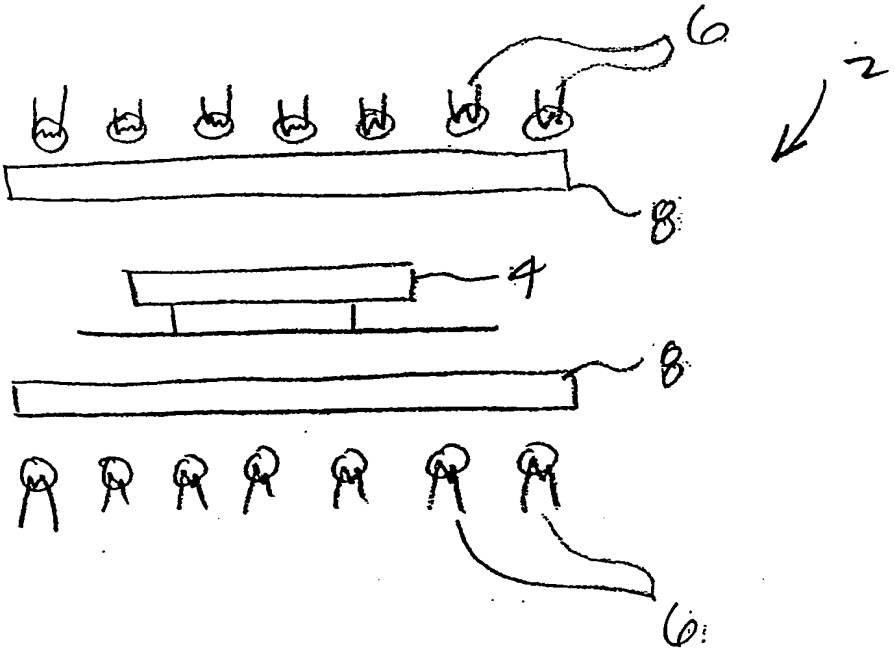


FIG_2

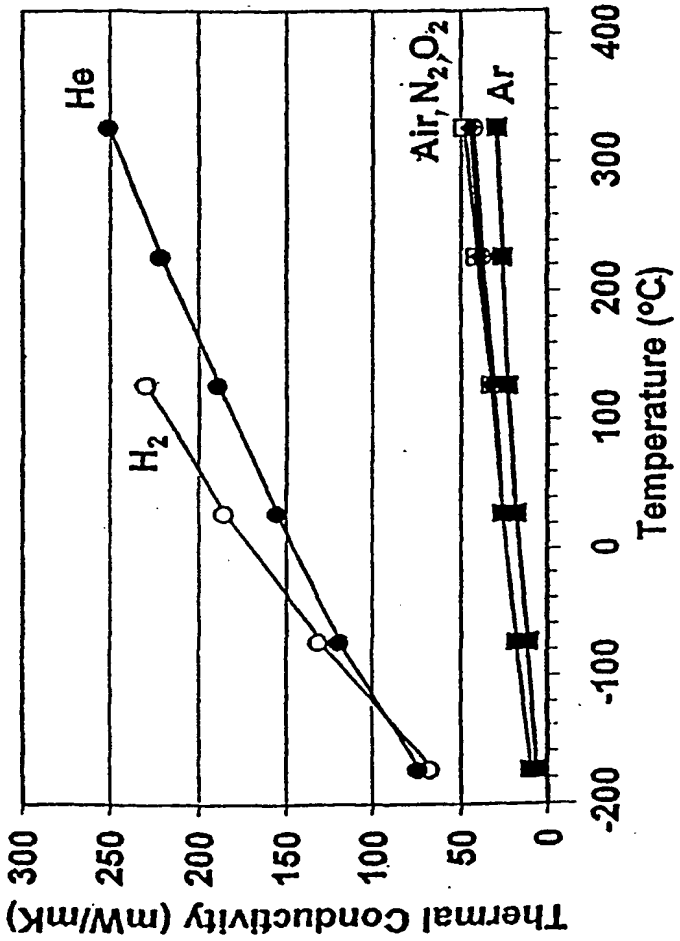

Thermal Conductivity (mW/mK)
300
250
200
150
100
50
0
Temperature (°C)
-200
-100
0
100
200
300
400
He
H2
Air, N2, O2
Ar

Fig-3

FIG. 4B

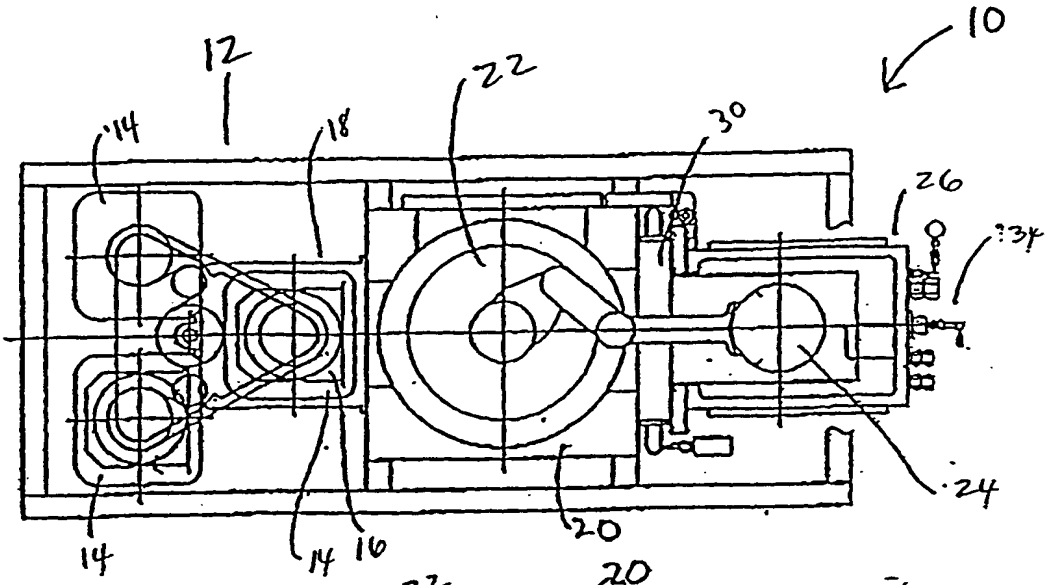
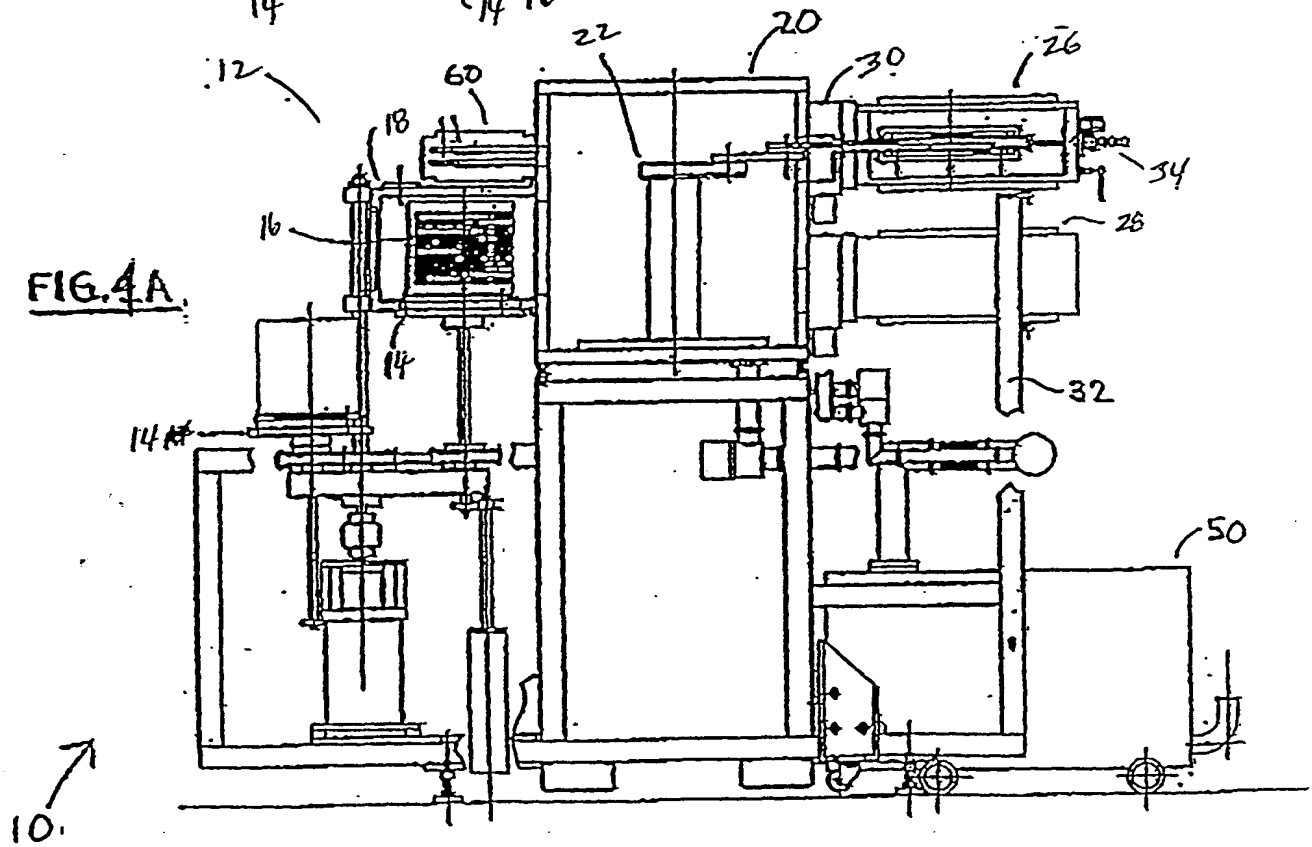


FIG. 4A



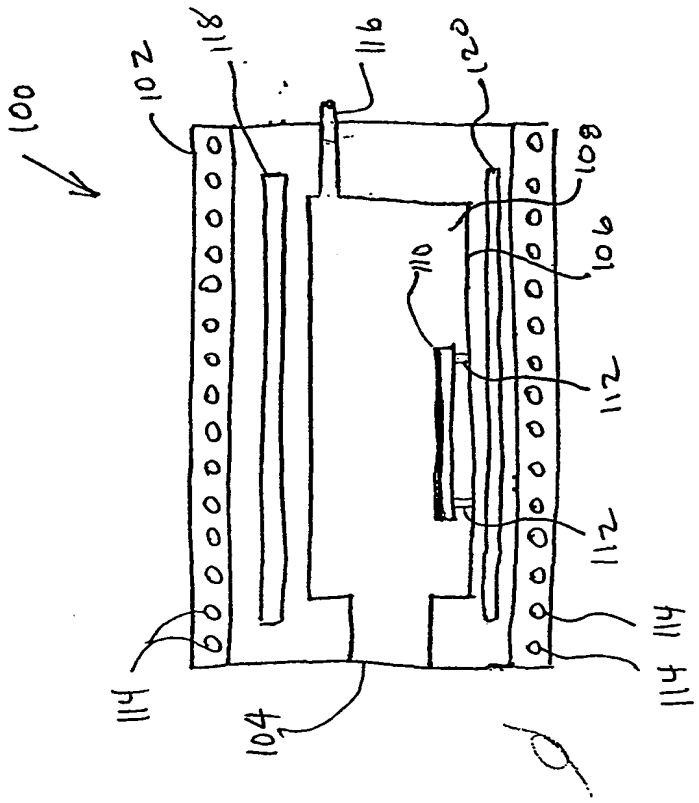


Fig - 5

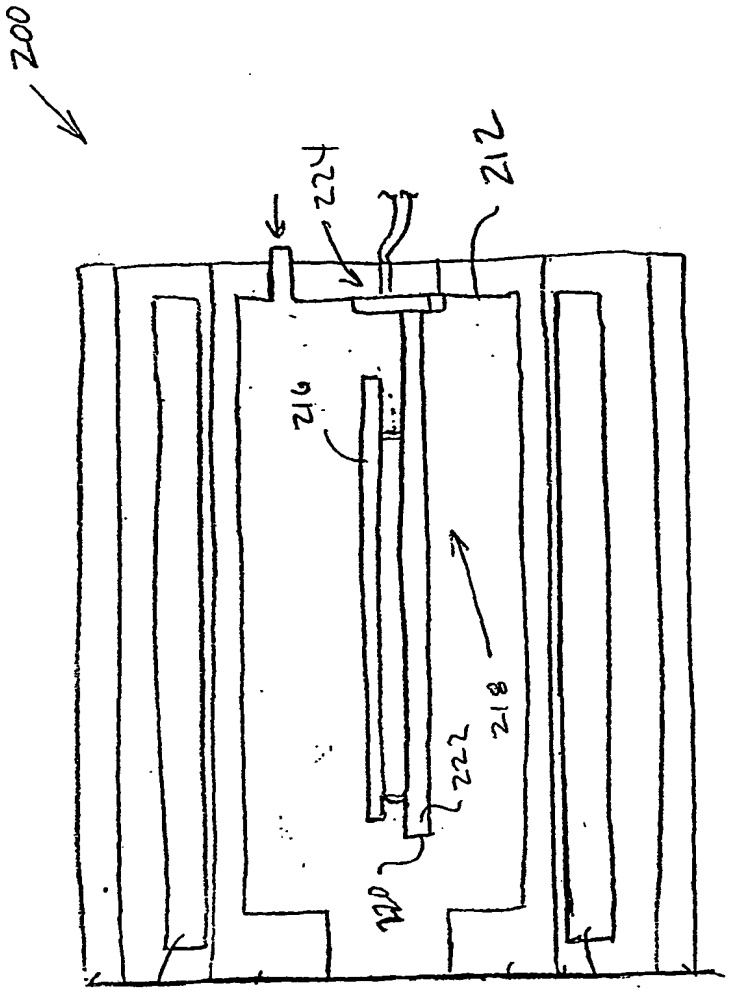
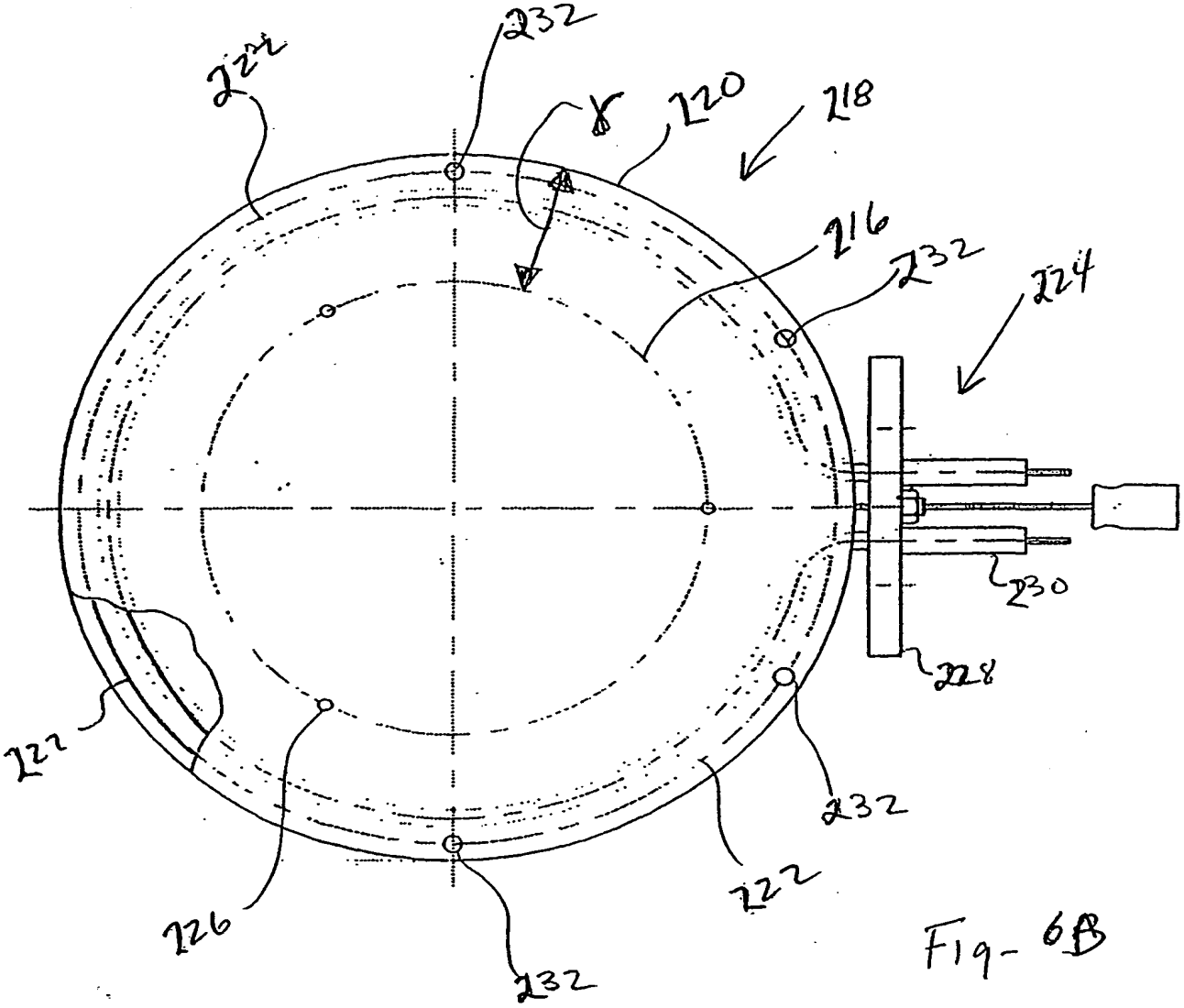


FIG- 6A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226
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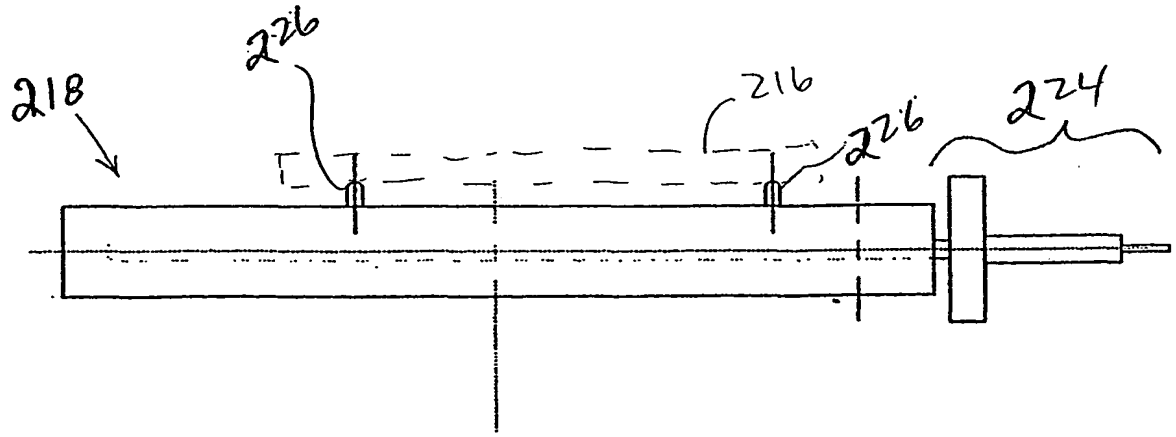
Fig- 6B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218
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Fig- 6C

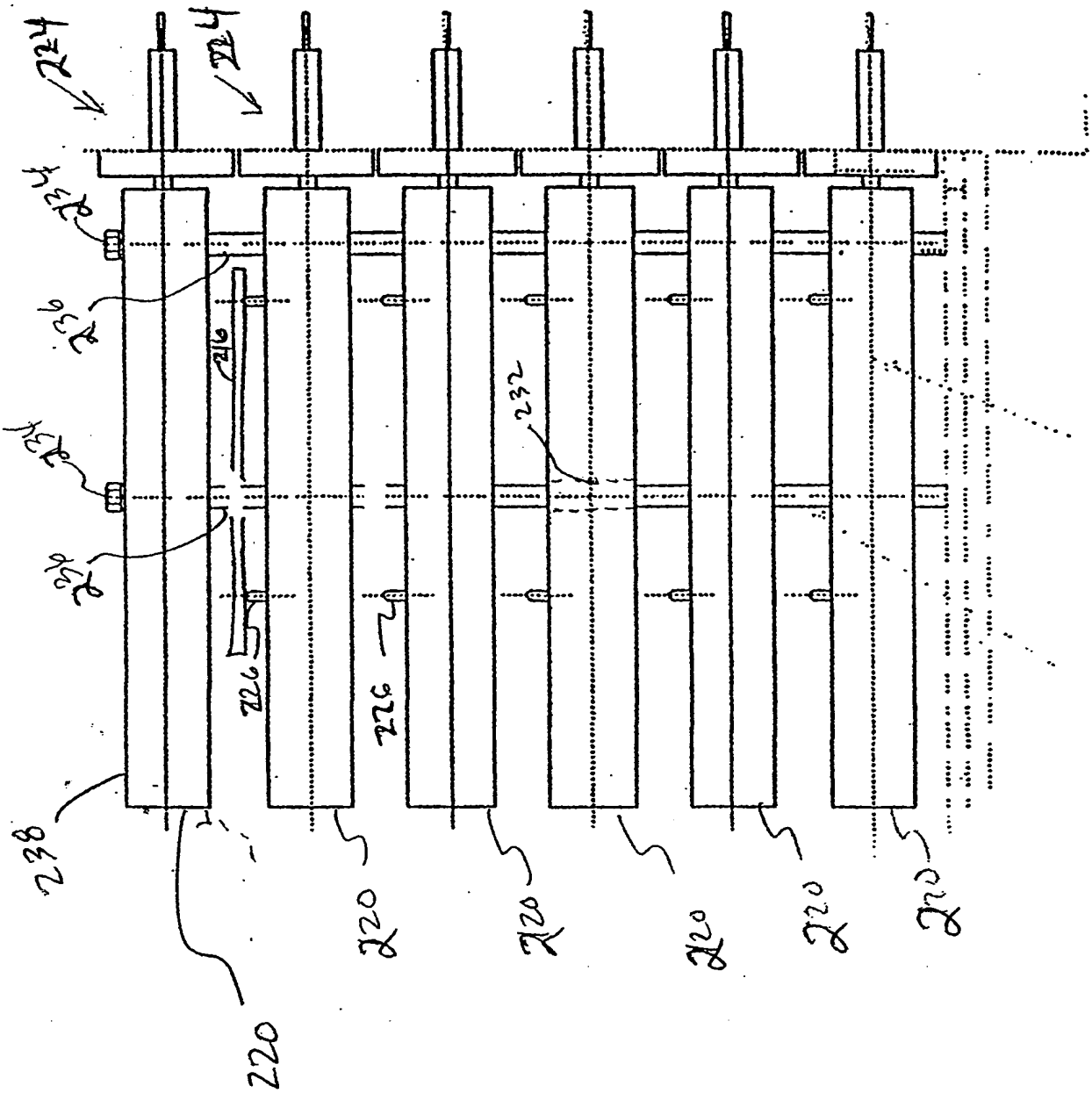
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Fig. 7

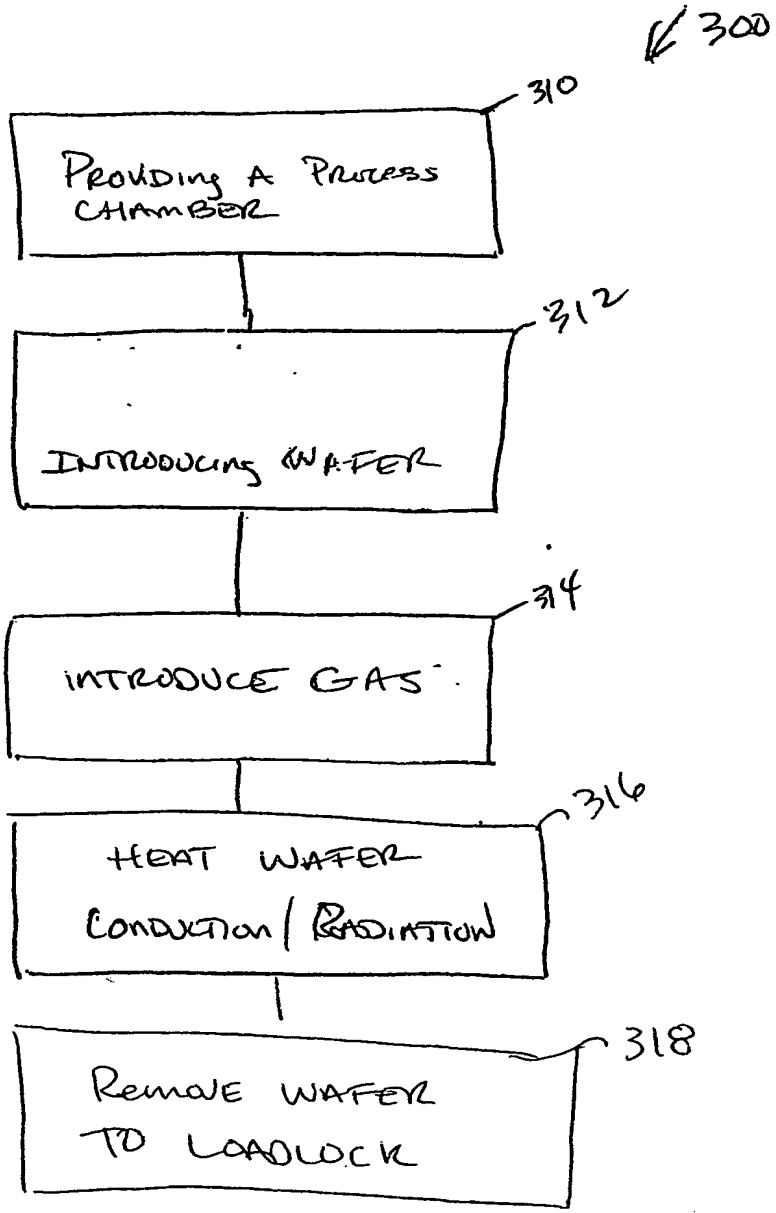
300
310
PROVIDING A PROCESS CHAMBER
312
INTRODUCING WAFER
314
INTRODUCE GAS
316
HEAT WAFER
CONDUCTION / RADIATION
318
REMOVE WAFER TO LOADLOCK

Fig - 8

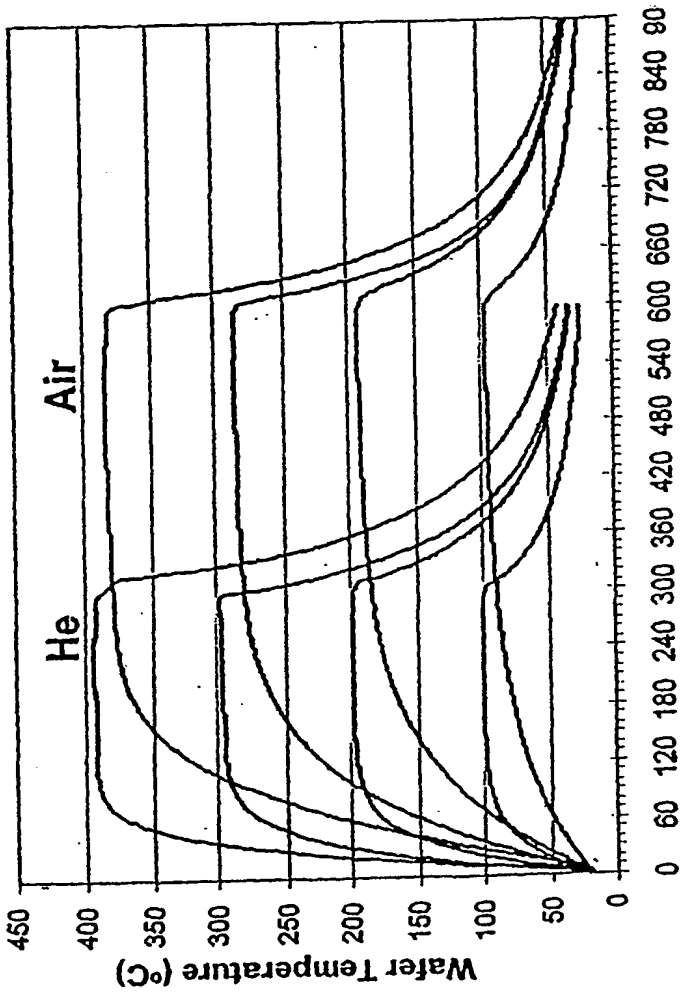
He
Air
Wafer Temperature (°C)
450
400
350
300
250
200
150
100
50
0
0 60 120 180 240 300 360 420 480 540 600 660 720 780 840 80
Time (s)

Fig 9

INTERNATIONAL SEARCH REPORT

Int onal Application No
PCT/US 01/12801

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 683 518 A (NISHIKAWA KATSUHITO ET AL) 4 November 1997 (1997-11-04)	1-4, 6-10, 12-17
A	column 9, line 30 - line 50 column 10, line 50 -column 12, line 18 column 21, line 40 - line 57 column 38, line 8 - line 39	5,11,18
X	US 5 881 208 A (JASINSKI THOMAS J ET AL) 9 March 1999 (1999-03-09) column 1, line 25 - line 40 column 4, line 62 -column 6, line 4 column 8, line 16 - line 33 column 9, line 35 -column 10, line 28	1-4,6,8, 16,17,19

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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28 August 2001	04/09/2001

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 298 314 A (SAMSUNG ELECTRONICS CO LTD) 28 August 1996 (1996-08-28) page 3, line 16 -page 4, line 24 page 6, line 17 - line 22 page 7, line 15 -page 10, line 3	1-4,6, 8-10, 13-17,19
X A	EP 0 419 302 A (FUJITSU LTD) 27 March 1991 (1991-03-27) column 3, line 55 -column 4, line 24 claims 5,7,8	1-3,6 16
A	EP 0 926 719 A (CANON KK) 30 June 1999 (1999-06-30) page 7, line 31 - line 39 page 10, line 35 -page 11, line 14	1-20
A	US 5 936 829 A (MOSLEHI MEHRDAD M) 10 August 1999 (1999-08-10) column 8, line 50 - line 64	1-20

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INTERNATIONAL SEARCH REPORT

formation on patent family members

Inte onal Application No
PCT/US 01/12801

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5683518 A	04-11-1997	US 5444217 A	22-08-1995
		US 5580388 A	03-12-1996
		US 5820686 A	13-10-1998
		EP 0633997 A	18-01-1995
		JP 7505261 T	08-06-1995
		WO 9417353 A	04-08-1994
		US 5710407 A	20-01-1998
		US 6151447 A	21-11-2000
US 5881208 A	09-03-1999	NONE	
GB 2298314 A	28-08-1996	GB 2293486 A	27-03-1996
		JP 8070008 A	12-03-1996
EP 0419302 A	27-03-1991	JP 3077329 A	02-04-1991
		DE 69004201 D	02-12-1993
		DE 69004201 T	03-03-1994
		US 5061642 A	29-10-1991
EP 0926719 A	30-06-1999	AU 9818498 A	15-07-1999
		JP 11251563 A	17-09-1999
		US 6171982 B	09-01-2001
US 5936829 A	10-08-1999	DE 19781631 T	01-04-1999
		GB 2325939 A	09-12-1998
		JP 2000505152 T	25-04-2000
		WO 9829704 A	09-07-1998